APPENDIX: PENDING CLAIMS

1. A circuit comprising:

a differential sense circuit;

a latch, said latch comprising cross coupled inverters;

said differential sense circuit and said latch being coupled so as to form a differential sense latch such that, in operation, an electronic signal stored in said latch is retained for at least one clock cycle.

3. The circuit of claim 1, further comprising a sense amp, said sense amp and said differential sense latch coupled such that, in operation, differential signals present on differential output terminals of said sense amp cause an electronic signal to be stored in said differential sense latch.

4. The circuit of claim 3, wherein said sense amp comprises a p-type sense amp.

5. The circuit of claim 4, wherein said differential sense circuit comprises:

a first inverter and a second inverter, said first and second inverters each having an input terminal and an output terminal, said input terminal of said first and second inverter being coupled respectively to a pull-down terminal, said output terminal of said first and second inverters being coupled respectively to a pull-up terminal, said output terminal of said first and second inverter being respectively coupled to opposite terminals of said latch, said input terminal of said first and second inverter being respectively coupled to a non-inverted output terminal and an inverted output terminal of said p-type sense amp;

a third inverter having an input terminal and an output terminal, said input terminal being coupled to said inverted output terminal and said output terminal being coupled to said pull-up terminal coupled to said first inverter; and

a fourth inverter having an input terminal and an output terminal, said input terminal being coupled to said non-inverted output terminal and said output terminal being coupled to said pull-up terminal coupled to said second inverter.

6. The circuit of claim 5, wherein said inverters comprise transistors coupled so that, in operation, substantially equivalent loads are applied to said inverted and non-inverted output terminals of said p-type sense amp.

7. The circuit of claim 3, wherein said sense amp comprises an n-type sense amp.

8. The circuit of claim 7, wherein said differential sense circuit comprises:

a first inverter and a second inverter each having stacked n-devices, an input terminal, an output terminal and a clock terminal;

said output terminals being coupled, respectively, to opposite terminals of said latch, said input terminals being coupled, respectively, to a non-inverted output terminal and an inverted output terminal of said n-type sense amp; and

said clock terminals being coupled to a pre-charge clock terminal of said n-type sense amp, wherein said clock terminals of said first and second inverters are further coupled to a respective top n-device of said stacked n-devices in said first and second inverters.

9. The circuit of claim 8, wherein said inverters comprise transistors which, in operation, represent substantially equivalent loads to said inverted and non-inverted output terminals of said n-type sense amp.

10. The circuit of claim 1, further comprising a differential domino circuit, said differential domino circuit and said differential sense latch being coupled such that, in operation, differential output signals present on differential output terminals of said differential domino circuit cause a corresponding electronic signal to be stored in said differential sense latch.

11. A method for storing electronic signals produced by a differential circuit comprising:

pre-charging said differential circuit;

evaluating said differential circuit;

sensing differential output signals via a differential sense circuit, wherein said differential sense circuit is coupled to a latch in a push-pull configuration; and

storing an electronic signal corresponding to said differential output signal.

12. The method of claim 11, wherein pre-charging said differential circuit comprises charging said differential output terminals to substantially the same voltage.

13. The method of claim 12, wherein said voltage comprises approximately ground.

14. The method of claim 13, wherein evaluating said differential circuit comprises:

applying a clock signal to said differential circuit at a substantially pre-determined point in time after said pre-charging; and

charging one of said differential output terminal to a voltage comprising approximately a power supply voltage.

15. The method of claim 12, wherein said voltage comprises approximately a power supply voltage.

16. The method of claim 15, wherein evaluating said differential circuit comprises:

applying a clock signal to said differential circuit at a substantially pre-determined point in time after said pre-charging; and

discharging one of said differential output terminals to a voltage comprising approximately ground.

17. An integrated circuit (IC) comprising:

a plurality of datapaths, at least one of said datapaths comprising:

a differential circuit and a differential sense latch, wherein said differential sense latch comprises a differential sense circuit and a jam-latch coupled such that, in operation, an electronic signal based, at least in part, on differential output terminals of said differential circuit is stored in said jam-latch.

18. The IC of claim 17, wherein said differential circuit comprises a sense amp.

19. The IC of claim 17, wherein said differential circuit comprises a differential domino circuit.

20. The IC of claim 17, wherein said jam latch comprises cross-coupled inverters.

21. The IC of claim 17, wherein said IC comprises a processor.

22. The IC of claim 21, wherein said processor comprises a microprocessor.

23. The IC of claim 21, wherein said processor comprises a network processor.

24. The IC of claim 21, wherein said processor comprises a digital signal processor (DSP).

25. The circuit of claim 1, wherein said differential sense circuit is coupled to said latch in a push-pull configuration.